PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Hans Boeve	Examiner:	Hien N. Nguyen
Serial No.:	10/579,933	Group Art Unit:	2824
Filed:	May 19, 2006	Docket No.:	**NL03 1361 US1**

Title: Method and Device for Performing Active Field Compensation During Programming of a Magnetoresistive Memory Device

Declaration Under 37 C.F.R. § 1.131

I, Hans Boeve, hereby present the following declarations.

Before April 22, 2003, while working alone (I being employed at Koninklijke Philips Electronics, N.V.).

1. I invented a method and device for providing compensation for the presence of an external magnetic field during programming of a magnetoresistive memory device such as an MRAM device.

2. I prepared and submitted an Invention Disclosure Statement having a two page form with a six page attachment. This invention disclosure statement provides details of the solving the challenges of the influence of an external magnetic field in the vicinity of the MRAM array during MRAM operation through the use of active field compensation. As disclosed and exemplified in the present application, there is an array of magnetoresistive memory elements comprising a source to apply a current or a voltage for generating a programming magnetic field at a selected magnetoresistive memory element. A magnetic field sensor unit measures an external magnetic field in the vicinity of the selected magnetoresistive memory element. A compensation circuit tunes the current or voltage for compensating locally for the measured external magnetic field during a programming operation. As further exemplified in the present application, I disclosed a method for compensating for the presence of an external magnetic field

during programming of a magnetic memory element, the programming being performed by applying an current (I_{bit}, I_{word}) or a voltage for generating a programming magnetic field to the magnetic memory element. The method comprises measuring the external magnetic field in the vicinity of the magnetic memory element and locally compensating for the external magnetic field during the programming operation by tuning the current (I_{bit}, I_{word}) or voltage for generating the programming magnetic field.

3. This invention disclosure statement was submitted to the Intellectual Property Department before April 22, 2003, and subsequently used to in the preparation of the above-referenced patent application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signed this 9th day of January 2008 by: ______________________
Hans Boeve

Invention Disclosure

This form and an annex containing a detailed description of the invention should be forwarded to Mr. Nico van Barschot, Tel. + 31 40 27 44308, Philips Intellectual Property & Standards, building WAH, Prof. Holstlaan 6, 5656 AA Eindhoven, The Netherlands. nico.van.barschot@philips.com.

Date:	Business Unit	To be filled in by Philips Intellectual Property & Standards
Date Redacted	Nat.Lab.	Date: Date Redacted ID-number: 613678

Names and first names of the inventors.	Sal. nr./ Empl. nr.	AfdNr	PostAddress	Email	Tel.
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Title of the invention Active field compensation during MRAM-write.	
Summary of the invention: An analog field sensor is added to a MRAM chip, and its output is used to tune the current levels during a write operation to be able to compensate for potential external magnetic fields. This way, the current levels used during a write operation follow the stable write field regions that shift with the external magnetic field.	
Detailed description of the invention on annexes; please describe preferred embodiments and their advantages over prior solutions in detail; please include drawings. (See page 2)	
Stage and importance of the invention a Stage of the invention?	☒ Research ☐ Pre-development ☐ Development ☐ (trial) manufacture
b In what products, processes or systems could the invention be used?	Any MRAM application, stand-alone or embedded (SoC), in particular for 'mobile' applications such as smartcards, mobile phones, PDA's, ...
c Which projects are related to the invention?	2002-082 New Initiatives in Magnetic Devices (++) 1999-065 Magnetic RAM technology for non-volatile memories (+)
d For which other business units of Philips could the invention have relevance?	CTO Chief Technology Office (++) ID Identification (+) PS Gen. General / Unspecified (+)
e For which competitors of Philips could the invention have relevance ? Why?	MRAM developers such as IBM, Motorola, Infineon, NEC, HP, Samsung, ... Potential MRAM customers in the 'mobile' application area such as smartcards, mobile phones, PDA's, ...
f For which LRTO(s) could the invention have relevance?	MAT Materials & Processing (++) SDT Silicon Device Technology (+)
Distribution of information concerning the invention When, how and where will information concerning the invention be distributed outside Philips? Please consider publications, hearings, exhibitions, offers, contacts with potential customers or suppliers, issuing of samples. **N.B. Even after sending this Invention Disclosure to Philips Intellectual Property & Standards, any such acts will impair patentability of the invention. Please contact Philips Intellectual Property & Standards before information concerning the invention leaves Philips.**	-
Supplemental information concerning the invention a Is the invention the result of a cooperation with persons outside Philips? If so, with whom?	-
b Is there, or will there be, an internal report on the invention? If so, please state the number.	-
c Are there, or will there be, other invention disclosures relating to this invention? If so, please state Ref.no.	Text Redacted
d Are there other persons who could give information on the invention? If so, who?	-
Recommendation Inventor as to urgency, commercial importance, and competitors' activities.	Text Redacted

PHILIPS

Attachments

WK-active field compensation.doc

IP&S imported Data		
a.	Patent Engineer:	
b.	Invention Source	
c.	Country of Invention	
d.	How important is the invention for the intended product(s) / service(s)?	
e.	What is the expected annual market size in five years from now that could use your invention?	
f.	Will the invention be proposed for an industry standard?	
g.	Is it possible to detect use of the invention by a competitor?	
h.	Additional information on the importance of the invention	
i.	Non Research Projects	
j.	Gevorment and/or university contracts	
k.	Third party cooperations	

- CONFIDENTIAL -

ACTIVE FIELD COMPENSATION DURING MRAM-WRITE.

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1. Introduction

Magnetoresistive random access memories are being aggressively developed in the Text Redacted as unified non-volatile memory technology of the future. The storage node consists of a magnetic tunnel junction, having two stable magnetization states, which can be addressed using arrays of bit and word lines. At zero magnetic field, the stable magnetization states, i.e. parallel and antiparallel alignment of the free storage layer with respect to a reference layer, have a large difference in resistance. Reading is done through a series transistor to avoid sneak currents through other elements. During a write operation, the bit state can be changed in a local magnetic field, generated by currents in the bit and word lines. Note that two magnetic field components are used to differentiate between the selected bit and other elements. The Figures 1 and 2 on the next page give some further information on the MRAM operational principle.

The switching curve of an element can be represented by its so-called astroid curve as shown in Figure 2 (upper left). The astroid curve unambiguously separates switching and non-switching events. In other words, if a field is being applied within the astroid, elements will not switch and maintain in their state, whereas fields exceeding the astroid may switch the element, if the previous state were the opposite one. Therefore, only if two magnetic field components are present, the bit state can be switched.

2. Problem

As disclose Text Redacted he influence of an external magnetic field in the vicinity of the MRAM array during MRAM operation can lead to different problems, whether shielding is present or not. We consider the effect of an external field on reading of data, writing operations, and data retention.

Reading of data: As long as magnetic fields are reasonably small, no issues are expected. The presence of a magnetic field may lead to a slight loss of signal due to small changes in magnetic alignment of memory devices. However, from the very square resistance / field loops obtained for deep sub-micron devices, we know that this effect will be small, before ultimately the alignment in the device would switch, which would result in loss of data. Therefore, we do not longer consider the influence of an external magnetic field on read operation. However, a constraint for any further measures or compensation schemes is that they have to allow for read operations.

Writing of data: A first magnetic **field threshold 1** is related to the margins of the current windows for writing. This margin will only be a few Oe, e.g. 5% margin on a switching field of 50 Oe would result in an absolute margin of only 2.5 Oe. Above this threshold,

write operations are dangerous, and may lead to non-intended bit-switching in non-selected neighboring devices.

Data retention: When the memory matrix is exposed to too high a field, loss of data may be the consequence. The **field threshold 2** corresponds to the minimum astroid curve of the memory matrix, taking into account process variations. Note that the field threshold 2 may be different for magnetic fields applied along different directions. A device to 'measure' this phenomenon was disclosed Text Redacted

3. Solution: active field compensation

Solutions for (local) active field compensation during write operation on a selected memory bits are disclosed. Figure 3 shows the effect of an external magnetic field on the astroid switching curve of a typical memory element. A feedback mechanism can be related to the output of a magnetic field sensor. Note that for active field compensation, an analog sensor is required. The magnetic field in the vicinity of the memory matrix can be measured in various ways, either 'directly', or 'indirectly'. The first (direct) method requires a sensor in the vicinity of the memory matrix, which is ideally based on the same technology. An example is disclosed Text Redacted , where analog sensors are created from the MRAM stack by rotating the shape over 90 degrees, by which orthogonal biasing arises. For conventional MRAM stacks, this will yield a good sensor device. Magnetic field sensors can also be incorporated in the MRAM system in a hybrid way (indirect measure).

The sensor output is used as a direct signal for the local, external magnetic field. For a reliable write operation, we have to locally compensate for the magnetic field. Text Redacted describes an active shielding based on the utilization of write lines for MRAM elements. However, write (as well as read) operations are not longer possible. In other words, data retention may be guaranteed, but read and write memory operations MUST be temporarily disabled. The only option available to allow for reading would be to add an extra bit line (on top of the existing bit line), and for write operations, also another word line should be added (below the existing word line, cfr Figure 1). From an integration point of view this mat be not acceptable. Therefore, the magnetic field has to be effectively compensated in the magnetic field generation during a write operation. In other words, the currents used during a write operation must be 'tuned' when a magnetic field would be present.

I present a simple current tuning schematic, based on the analog sensor input. Note that the sensor(s) or sensor system must give a 2D description of the magnetic field in the vicinity of the MRAM array. The effect of the external magnetic field on the astroid curve, as well as the required field windows is depicted in Figure 3 for a (negative!) external magnetic field being applied along the 45° direction. The 'field threshold 2' is shown as the red astroid-like curve. In practice, a simple current tuning scheme can be incorporated for fields below this 'field threshold 2'. As a matter of fact, other currents have to be applied in order to manipulate the data bits now. As it is not straightforward to

apply a compensating magnetic field, which would shift the astroid back to zero-field, the only option remaining is to tune the current levels in such a way that the required field window for write operation is shifted along with the measured external field.

In a **first embodiment**[1], the sensor output is directly used as input to a novel block with as function to generate the two compensation currents for the bit and word field (I_{comp_b} and I_{comp_w}, respectively), i.e. easy and hard axis field, as shown in Figure 4. The current sources I_{comp_b} and I_{comp_w} must be bipolar, and ideally able to correct for any field between e.g. 'field threshold 1' and 'field threshold 2'. Note however that in the case of an external magnetic field close to field threshold 2 being present, the current needed for writing may in certain cases nearly double, which may have its implications to the highest current levels possible in the memory architecture, e.g. with respect to the electromigration limit. Moreover, compensation for fields exceeding 'field threshold 2' is in principle possible, but probably not realistic as retention of other memory bits can no longer be guaranteed. For too small fields, one may decide not to apply any current tuning, as the external fields falls within the write field margins.

Figure 5 gives an impression of all external fields that can be compensated for, e.g. along the 45 degree directions (upper graph), or the easy axis (lower graph). Note that the zero-magnetic field point, i.e. the origin of the graphs, always lies within the shifted astroid curves, to be able to tune the current levels. If not, 'field threshold 2' was be exceeded, leading to a possible loss of data retention. In practice, taking into account current limitations along the main axes, magnetic fields within the yellow area may be compensated for by current tuning.

In a **second embodiment**, the sensor output can be part of a direct feedback loop that is generating the required currents using magnetic field nulling along both the easy and hard axis. This active component forces the sensor(s) to remain in their zero-state by generating a magnetic field that exactly compensates for the external magnetic field in the sensor(s). As for MRAM cells, magnetic field generation is done using current lines under and/or on top of the sensor(s). If the geometry of the sensor(s) resembles that of the memory elements, this compensation current can then be directly fed into the MRAM array. In Figure 4, this is schematically depicted by the dashed feedback loop. The embodiment can be integrated as a continuous feedback loop (in time).

4. Summary

An analog field sensor is added to a MRAM chip, and its output is used to tune the current levels during a write operation to be able to compensate for potential external magnetic fields. This way, the current levels used during a write operation follow the stable write field regions that shift with the external magnetic field.

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[1] Text Redacted
Current tuning may be not such a difficult option as I initially guessed. It may therefore be important to claim a simple analog sensor feedback-system as a separate invention that is taking into account the possibility of an external field in the magnetic field pulse generation.

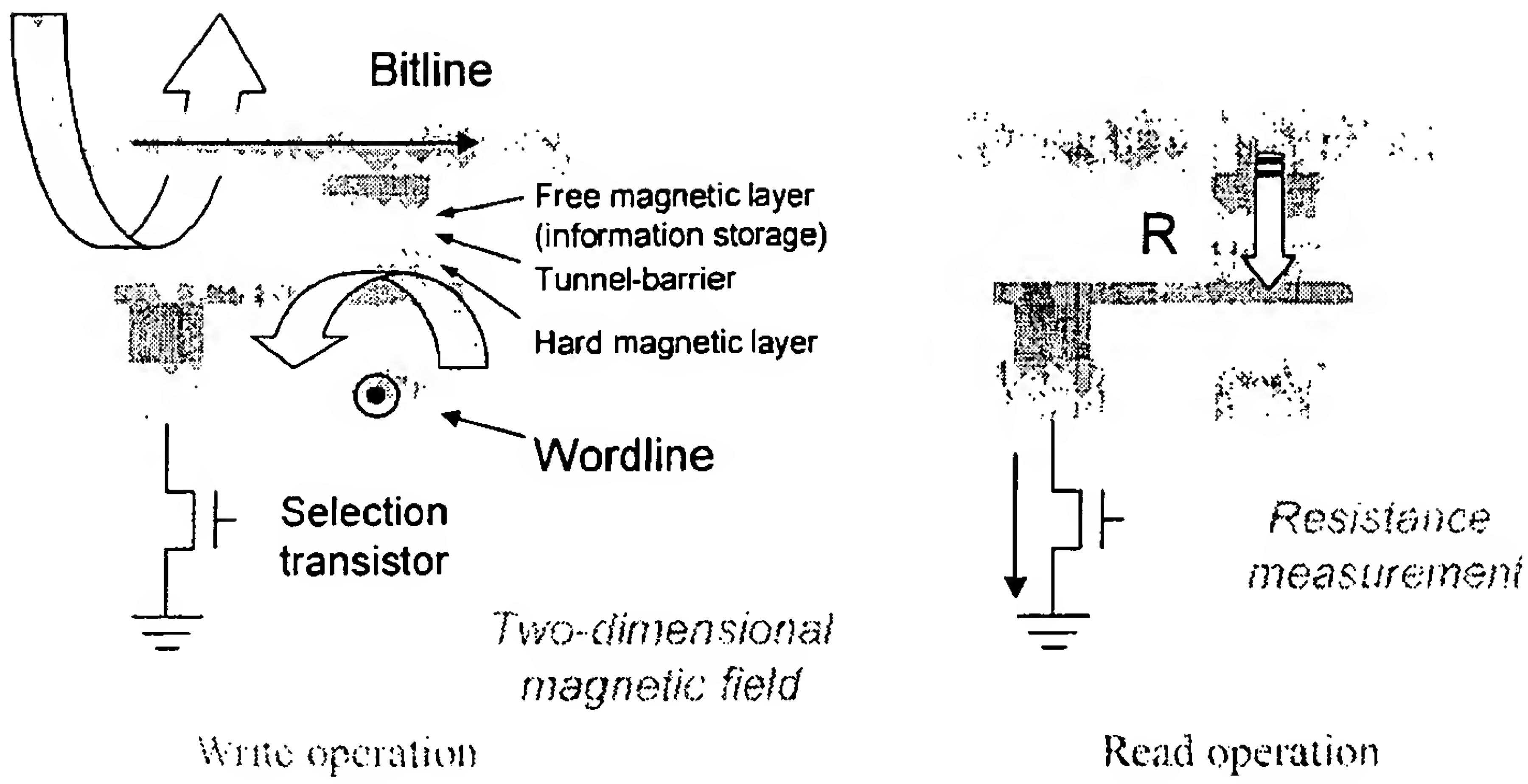

Figure 1: MRAM operating principle (write-read) for a 1T-1MTJ architecture.

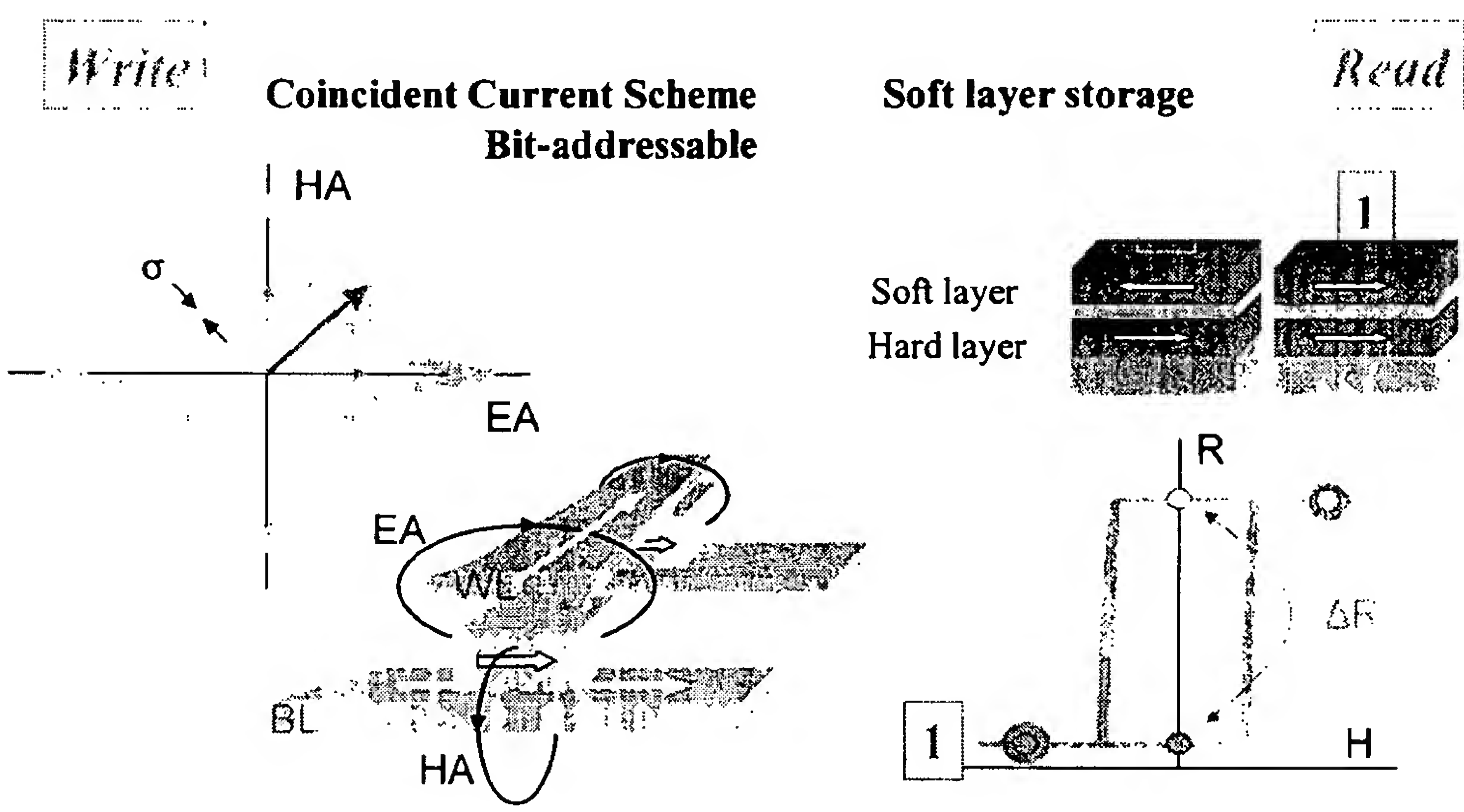

Figure 2: Write and read strategies for MRAM, in which the information is stored in the magnetization direction of the soft layer. During a write operation, bit-addressability is provided in the coincident current scheme as depicted in the astroid curve of the soft layer. Information is read by resistance, which basically compares the magnetization state in the soft and reference layer.

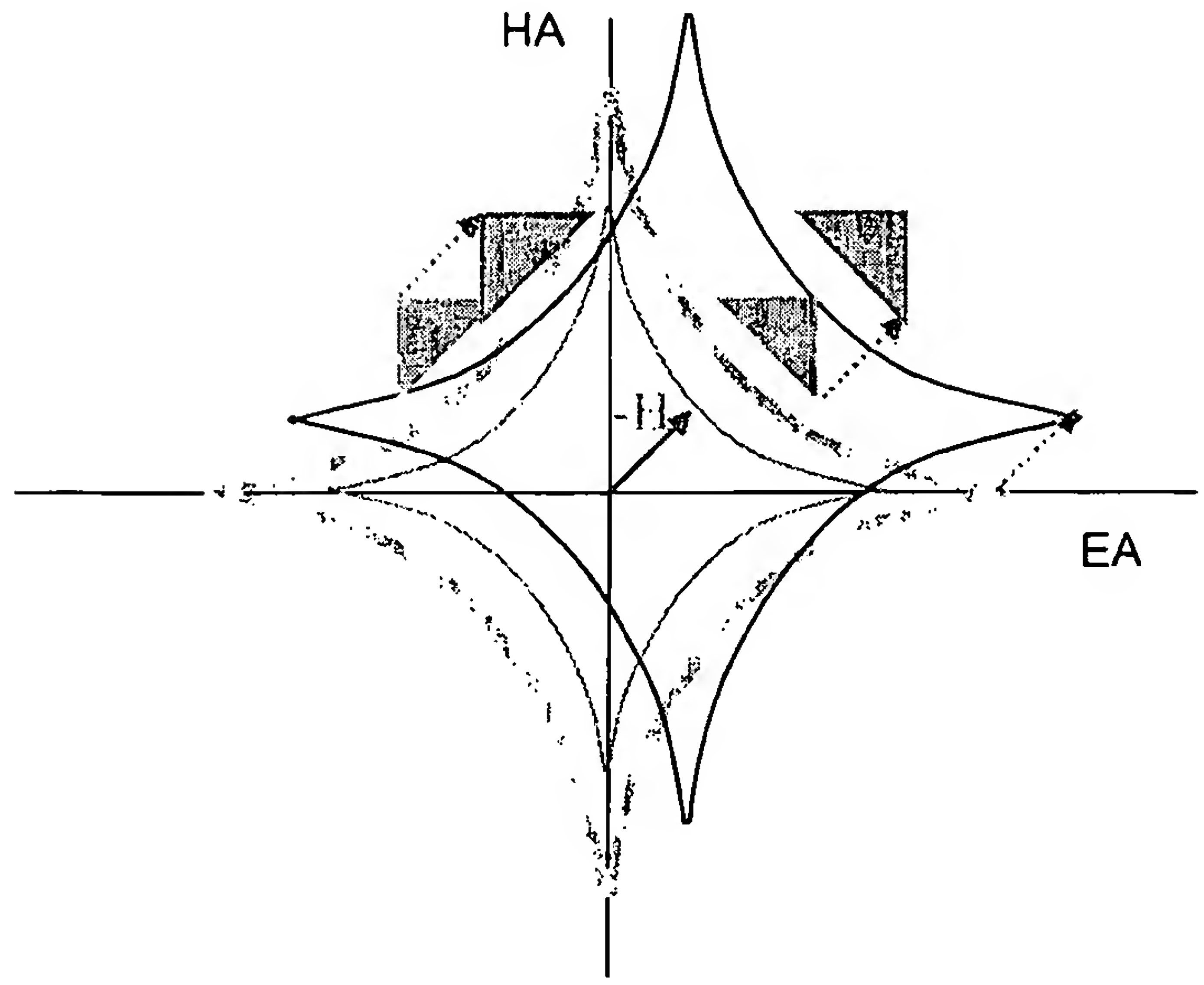

Figure 3: Shift of the astroid curve and current windows (triangles) due to an external field H (opposite direction). The 'field threhold 2' is represented by the smaller red astroid-like curve.

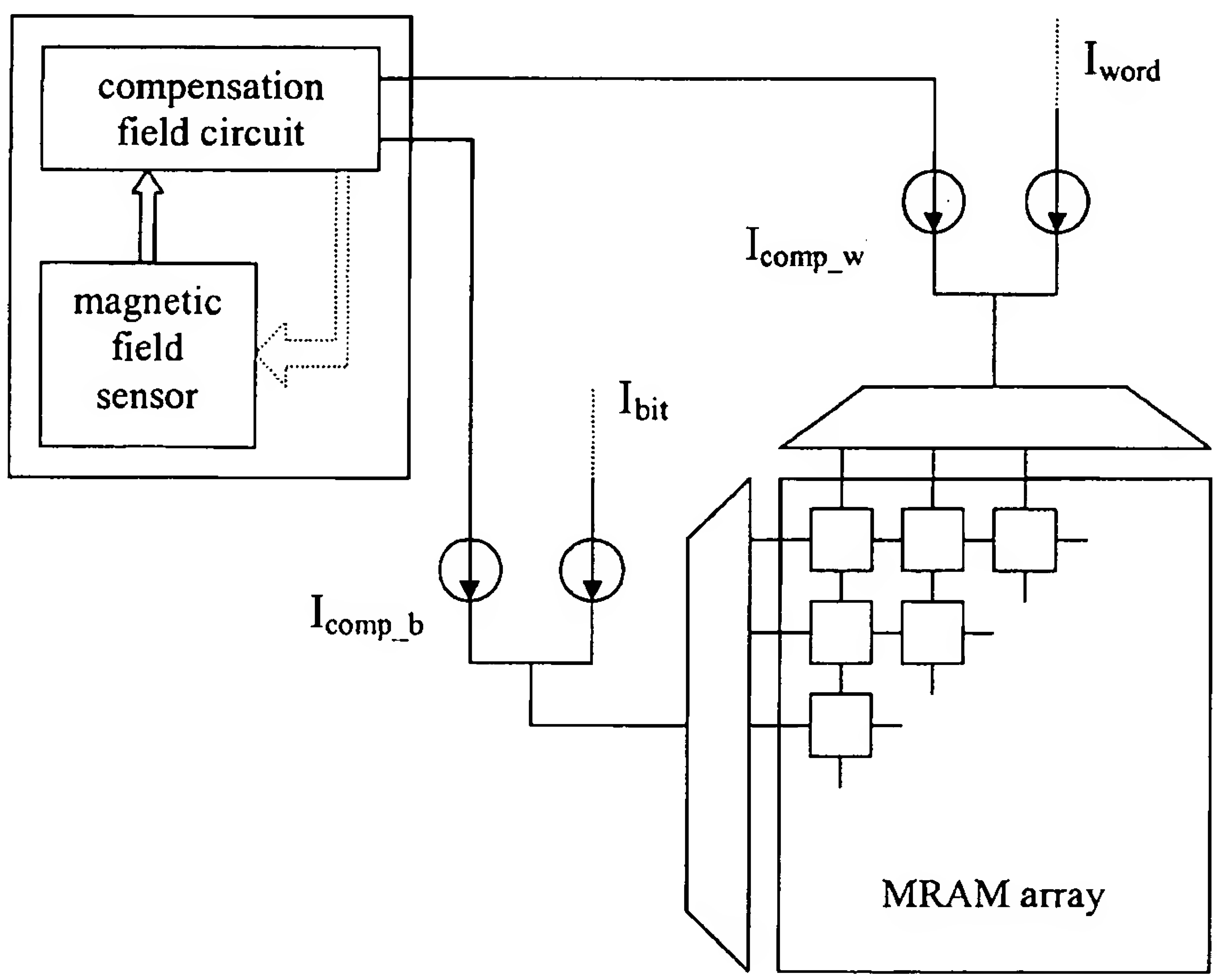

Figure 4: Schematic system for current tuning. Input from a magnetic field sensor is used in the compensation field circuit, which effectively may a zero-field feedback system (Embodiment 2), generating the compensation currents.

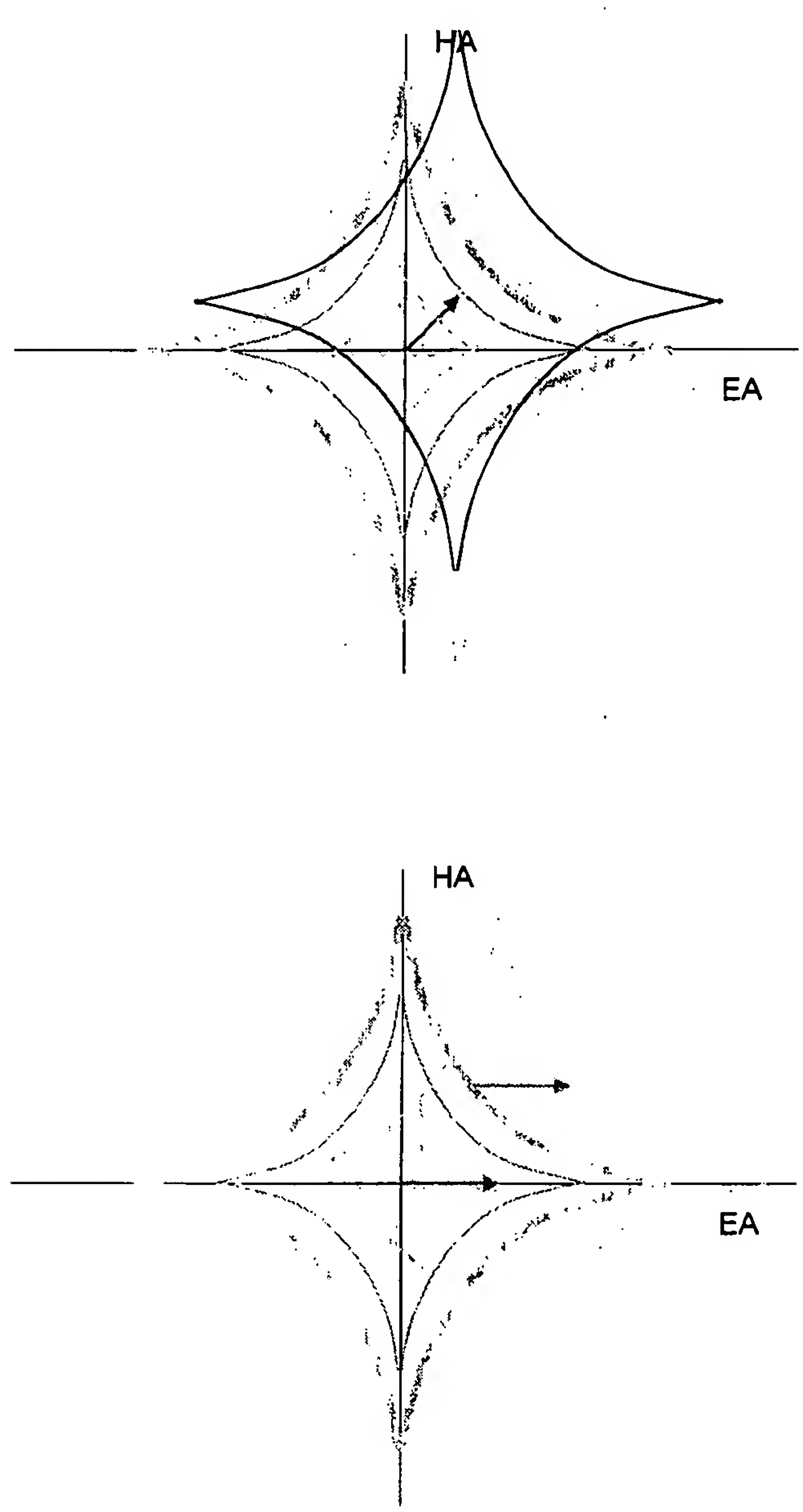

Figure 5: Schematical representation of fields that can be compensated for, (upper graph) example for fields under 45 degree with respect to main axes, (lower graph) along one of the main axes, i.e. easy axis. The yellow region represents the magnetic fields that can be compensated for.